Robustness and Security of Integrated Systems Infrastructure

Modern Systems-on-Chip (SoC) require the integration of a huge number of instruments. Trace buffers, testing interfaces, debuggers, sensors and monitors are just a few examples. They are needed for testing, debugging, maintenance as well as the continuous monitoring and reliability management of the system throughout its lifetime.

The integration of this large infrastructure into SoCs poses a huge challenge. On the one side, it is required to provide flexible and scalable access to the Infrastructure during the whole system lifetime. This requirement is fulfilled by the Reconfigurable Scan Networks, which were recently standardized by IEEE Std. P1687.

On the other side, this flexible access creates several challenges that need to be addressed for the robust and secure operation of the system throughout its lifetime. To name a few, managing the dependability of the chip using infrastructure, generating test patterns to find possible defects, diagnosis of the location of defects and the security of the data transmitted throughout this infrastructure.

The access structure of this infrastructure is too complex for conventional methods of dealing with these challenges. A lot of research is being done to create new architectures and algorithms that will enable the continued functionality, dependability, robustness and security of the integrated infrastructure throughout its lifetime.

Especially in safety-critical systems, such as automotive electronics, medical technique or Industrie 4.0, it is extremely important to have continuous, correct and secure functionality.

This seminar covers some of the most important challenges in context of:

- Modeling and verification for access to infrastructure
- Test methodology and Test pattern generation
- Diagnosis and fault localization
- Design rules and methods for secure access to On-Chip Infrastructure

Prior registration via ILIAS is required.

http://www.itil.uni-stuttgart.de/lehre/robustness

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