Embedded Systems Lab Course / Fachpraktikum

For the development of digital systems, modeling and simulation are important tools used in each development step at the necessary level of abstraction. In this simulation-centric lab, you will model, simulate, and synthesize digital circuits and systems using state of the art hardware description languages and modeling styles for various abstraction levels.

The lab is organized in two parts. The first part deals with modeling, simulation and synthesis of digital circuits using VHDL. Behavioral and structural modeling styles will be addressed as well as synthesizable description styles such as for finite state machines and datapaths.

The second part focuses on the system level by modeling and simulating complete digital systems using SystemC and Transaction Level Modeling (TLM). Starting with behavioral models communicating via signals, we will increase system complexity and raise the abstraction levels towards modeling of component interactions using transactions as defined by the TLM 2.0 standard.

Prerequisites
The following prerequisites are mandatory for participation in this lab:

- Experience with the C++ programming language, object oriented programming (OOP), and the Unified Modeling Language (UML).
- Prior attendance of RO/TI2 or any other course on digital circuits and computer organization, e.g. a passed bachelor course.

Entry Test
On the first date, there will be a short, written test to determine your eligibility. The test will take about 30 minutes and cover the prerequisites. By attending, students on the waiting list have the chance to get into the course if other students drop out.